(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 559 366 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
10.12.1997 Bulletin 1997/50

(51) Int Cl.[6]: **H01L 25/10**, H01L 25/065

(21) Application number: **93301336.9**

(22) Date of filing: **23.02.1993**

(54) **Stackable three-dimensional multiple chip semiconductor device and method for making the same**

Dreidimensionale gestapelte Mehrchip-Halbleiteranordnung und Verfahren zum Herstellen derselben

Dispositif semi-conducteur à puces multiples empilées à trois dimensions et procédé de sa fabrication

(84) Designated Contracting States:
DE FR GB IT

(30) Priority: **02.03.1992 US 844075**

(43) Date of publication of application:
08.09.1993 Bulletin 1993/36

(73) Proprietor: **MOTOROLA, INC.**
Schaumburg, IL 60196 (US)

(72) Inventor: **Lin, Paul T.**
Austin, Texas 78731 (US)

(74) Representative: **Gibson, Sarah Jane et al**
Motorola
European Intellectual Property Operations
Midpoint
Alencon Link
Basingstoke, Hampshire RG21 7PL (GB)

(56) References cited:
EP-A- 0 377 932

- **PATENT ABSTRACTS OF JAPAN vol. 5, no. 44 (E-50)(716) 24 March 1981 & JP-A-55 165 661**
- **RESEARCH DISCLOSURE no. 313, May 1990, EMSWORTH,GB page 372 'organic card device carrier'**

EP 0 559 366 B1

Printed by Jouve, 75001 PARIS (FR)

Description

Field of the Invention

The present invention relates to semiconductor devices in general, and more specifically to stackable three dimensional semiconductor multiple chip modules.

Background of the Invention

Most large scale integrated circuits (ICs) are presently packaged in plastic or ceramic packages with metal leads extended therefrom for soldering to a printed circuit (PC) board or for insertion into a socket. Typically, these IC packages are configured as dual-in-line or quad-flat packages. In most instances only a single IC is contained within a package, although multiple chips are sometimes contained within a package. The circuit density resulting from this packaging technology is not very great since the ceramic or plastic package consumes relatively large areas of the mounting surface, usually a printed circuit board, particularly if a socket is used.

Moreover, printed circuit boards, like everything else in electronics, are getting smaller, faster and denser. A more compact packaging technology is needed when mounting area is limited or when speed considerations dictate that circuit elements be closely spaced. One such technology comprises the use of a cofired ceramic substrate onto which ICs in an unpackaged form are directly attached to the ceramic mounting surface and are wire bonded to conductive areas on the mounting surface, or are inverted and connected directly to metallized areas on the ceramic mounting surface by, for example, a solder-bump technique. This multiple chip module (MCM) technology has several limitations, however. Interconnecting multiple ICs on a single ceramic mounting surface requires deposition of a metallic material in a pattern which desirably avoids cross-overs. Furthermore, the deposition of metallic conductors of extremely fine resolution is difficult on many surfaces. Multi-layered interconnections are also possible but are sometimes prohibitively expensive and have limited thermal power dissipation capability under air cooling. Direct chip attach has a further limitation of no burn-in capability before module assembly and is difficult to repair after board mounting. Additionally, if components, whether active or passive, are necessary to the circuit, discrete components must be used with their attendant problems of size and mounting mechanisms.

Nevertheless, the advent of MCMs offers distinct advantages in the packaging of ICs. Time delay between chips is less; electrical noise and cross talk are less; and size is less. The chips used can be bigger, and the I/O lead counts have greatly increased per multiple chip module. Despite their various advantages, however, current MCMs have their own set of problems. Thermal management problems have become huge. Heat generated from multiple devices must be removed. As gates are crowded ever more densely on a chip, the entire thermal path, from die to die-attach to substrate to heat sink, should be taken into account. Single crystal silicon and high thermal conductivity ceramics such as aluminum nitride and silicon carbide have heat transfer and thermal averaging capabilities better than traditional ceramic and printed-circuit board materials. Temperature gradations also strongly influence the reliability of solder, wire bond, and electrical connection. In effect, to achieve a successful MCM design, a balance must be struck between materials having individually the most effective thermal conductivity and materials having as a group similar coefficients of thermal expansion.

Traditionally, all dice are probed individually before assembly, while critical units are burned in under accelerated aging conditions to minimize the risk of subsequent system failure. Burn-in is performed to screen out weak devices, and packaged devices rather than bare chips are normally burned-in. Most burn-in failures are device or die related due to weak gate oxide. Adapting burn-in to MCMs, this process should be performed at the packaged module level. The drawback in module level burn-in is that a percentage of die in the module will fail, and replacement with another good die has to be performed by proper removing procedure.

Another MCM approach interconnects bare chips not in the X-Y plane but along the Z-axis. Three dimensional packaging offers higher memory density and less required interconnect density than planar multiple chip substrates. Consequently, connection systems that link MCMs, discretes, and passives are expected to grow in the Z-direction, orthogonal to the substrate. Three-dimensional packaging of ICs offers advantages in numerous fields. For example, it can be useful in supercomputer memories where speed and densification are important, or in large cache memories where access time and densification are critical.

One method of interconnecting bare chips forms a cube of stacked chips. Chips are individually interconnected on a thin film identical to a TAB film by means of gold wires prior to cubing. After passing electrical testing and burn-in, they are then glued on top of one another with TAB film. A major disadvantage to this configuration is limited heat dissipation. Furthermore, once this cube of chips is formed and mounted onto a substrate, rework of subsequent chip failure is highly impractical, so redundant chips are included in the stack which adds to the overall cost of the module.

An ultradense MCM would ideally incorporate the planar multi-chip module with the three-dimensional approach. Stacking of Pin Grid Arrays (PGAs) to form an MCM has been in existence for two decades. A bottom substrate is provided with copper pins in a conventional manner. Semiconductor dice are then flip-chip mounted to chip carrier substrates. An interposer physically and electrically couples a chip carrier substrate to another chip carrier or to the bottom substrate by way of solder

joining the interconnections. These interconnections are located around the periphery of each substrate which could feasibly limit chip configuration and, therefore, chip density on each level. The copper pins of the PGAs and the interposers provide the stand-off between the carriers to keep them from collapsing onto each other.

Thus, power distribution, heat dissipation, and temperature, as well as testing, burn-in, and rework should all be taken into consideration in the successful design of MCMs. The difficulty in designing MCMs is finding and assembling materials with the right blend of electrical, mechanical, and thermal properties. Trade-offs are almost always required and typically depend on the application. A need exists for an easily manufacturable ultradense MCM which is cost effective as well as meeting all of the design criteria aforementioned.

JP-A-60194548 describes a method for stacking semiconductor devices whereby an upper part of a chip carrier body is provided with an electrode for stacking connection

Summary of the Invention

In accordance with a first aspect of the invention, there is provided a stackable semiconductor multiple chip module according to claim 1 comprising: a lower chip carrier substrate of thermally conductive material having a plurality of solder bumps on both top and bottom surfaces of the lower chip carrier substrate; a first semiconductor die electrically and physically attached to the lower chip carrier substrate; an upper chip carrier substrate of thermally conductive material having a top and a bottom surface; a plurality of solder bumps on the bottom surface of the upper chip carrier substrate; a second semiconductor die mounted and electrically coupled to the upper chip carrier substrate, wherein the lower chip carrier substrate and the upper chip carrier substrate are electrically connected to each other by solder joints; and a lid capping the first semiconductor die and serving as a positive stand-off to create hour-glass solder joints between the upper chip carrier substrate and the lower chip carrier substrate.

In accordance with a second aspect of the invention, there is provided a method as claimed in claim 7.

Brief Description of the Drawings

FIG. 1 is a cross-sectional view of a stacked three-dimensional semiconductor multiple chip module (MCM) prior to solder reflow, in accordance with the present invention.

FIG. 2 is a cross-sectional view of a stacked three-dimensional semiconductor MCM with a heat sink, illustrating an embodiment of the present invention.

FIG. 3 is a cross-sectional view of a semiconductor device mounted onto a chip carrier substrate with solder bumps on the lower surface of the substrate, which illustrates a step in assembling the three-dimensional semiconductor MCM, in accordance with the present invention.

FIG. 4 is a cross-sectional view of a semiconductor device mounted onto a chip carrier substrate with solder bumps on both the lower and upper surfaces of the substrate, which illustrates a step in assembling the three-dimensional semiconductor MCM, in accordance with the present invention.

FIG. 5 is a cross-sectional view of a stacked three-dimensional semiconductor MCM, illustrating an embodiment of the present invention.

FIG. 6 is a cross-sectional view of a stacked three-dimensional semiconductor multiple chip module with a lid over the lower semiconductor device, illustrating an embodiment of the present invention.

Detailed Description of a Preferred Embodiment

With the present invention, it is possible to meet the previously stated desired feature of a three-dimensional multiple chip module to densely package semiconductor devices without sacrificing board space in the X-Y plane. The invention enables a multiple chip module to be stacked in the Z-direction. Moreover, this invention provides a method for manufacturing such a module. In accordance with the invention a cross-sectional view of a stacking multiple chip module 8, prior to solder reflowing, is illustrated in FIG. 1. A semiconductor die 10 is mounted onto a lower chip carrier substrate 12. Electrical connections between semiconductor die 10 and lower chip carrier substrate 12 are made by wires 13 bonded in conventional fashion. Furthermore, semiconductor die 10 is encapsulated by an encapsulant 14, which can be of any conventional encapsulating material, such as a molding compound or glob top, or any other suitable material. Lower chip carrier substrate 12 is preferably formed from a thermally conductive material such as aluminum nitride or silicon. Printed circuit board material such as FR-4 can also be used although this material is not as thermally conductive as a ceramic or silicon. A large thermal expansion mismatch must also be considered when choosing PC board material. Its low cost, however, may be enough of an incentive to the user to accept.

Additionally shown in FIG. 1, the lower chip carrier substrate 12 has a plurality of solder bumps 15 on the bottom surface of the substrate. These solder bumps 15 are used to mount the lower chip carrier substrate 12 to the actual PC board, which is not shown. Furthermore, lower chip carrier substrate 12 also has a plurality of solder pads or bumps 16 on the top surface of the substrate. Solder pads 16 serve to join lower chip carrier substrate 12 to another chip carrier to be mounted above.

Also shown in FIG. 1 is another semiconductor die 18 mounted onto an upper chip carrier substrate 20. Electrical connections between semiconductor die 18

and upper chip carrier substrate 20 is made by wires 21 TAB bonded to the substrate. Furthermore, semiconductor die 18 is encapsulated by an encapsulant 22, which can be of any conventional encapsulating material, such as a molding compound or glob top, or any other suitable material. Upper chip carrier substrate 20 also has a plurality of solder bumps 23 on its bottom surface. When the lower chip carrier substrate 12 and upper chip carrier substrate 20 are properly aligned for solder joining, then the solder bumps 16 and 23 combine to form fine pitch solder columns.

In this embodiment, lower chip carrier substrate 12 and upper chip carrier substrate 20 have through-hole vias 24 to make electrical connections to each other and to other substrates. However, multi-layer chip carrier substrates could also be used for the same purpose of making electrical connections to another substrate.

Illustrated in FIG. 2 is a cross-sectional view of a stacking multiple chip module 25. Many of the features in this embodiment are the same as previously discussed in FIG. 1, and will, thus, be labeled accordingly. In this embodiment, the lower chip carrier substrate 26 has one semiconductor device 27 mounted thereon. A thermally conductive lid 28 caps the semiconductor device 27. Lid 28 can serve as a positive stand-off to create hour glass shaped solder joints 29. This hour glass shape maximizes the time to failure of the solder joints 29 due to fatigue stresses. The sizes of the solder bumps or pads 16 and 23, aforementioned in FIG. 1, need to be optimized according to lid height to achieve the hour glass shape of solder joints 29. Without a lid in place, the top and bottom solder bumps will coalesce during the solder reflow process to form larger single solder bumps. While this shape may be acceptable, the hour glass shape is more desirable for fatigue life. Upper chip carrier substrate 30 has two semiconductor devices 32 and 34 mounted thereon in a staggered configuration. A heat sink 40 is attached to the upper chip carrier substrate 30 where it can dissipate heat from the lower semiconductor device 27 through the thermally conductive upper chip carrier substrate 30 and lid 28. It should be noted that if a third level chip carrier is used, then the subsequent upper level semiconductor devices must also be staggered to allow a heat sink to be attached to dissipate heat away from the lower level semiconductor devices. A second heat sink 41 is mounted above heat sink 40 to form a stacked cooling fin configuration. It is entirely possible to add more heat sinks above heat sink 41 to increase the level of heat dissipation of the MCM, with the only limitation being the volume available above the PC board whereon the MCM is to be mounted.

Also in accordance with the present invention is a method for stacking chip carriers to create a three-dimensional MCM. Illustrated in FIG. 3 is a cross-sectional view of a partially populated chip carrier 42. As illustrated in FIG. 3, a semiconductor device 44 is mounted onto a chip carrier substrate 46. Chip carrier substrate 46 is illustrated to be multilayered. It should be noted that a chip carrier substrate in any of the embodiments can be multilayered or have through-hole vias to enable electrical connections of the device to a board. A plurality of solder bumps or balls 23 of a particular solder composition are then deposited onto the bottom surface of chip carrier substrate 46. This solder, for example, may be of an 80/20 Pb/Sn composition or any other workable solder alloy composition. Electrical connections are made between the semiconductor device 44 and solder bumps 23 via multi-layer interconnects 47. Chip carrier 42 can be tested and burned-in either before or after the deposition of solder bumps 23.

A cross-sectional view of a fully populated chip carrier 48 is illustrated in FIG. 4. A semiconductor device 50 is mounted on a chip carrier substrate 52. As illustrated in FIG. 4, semiconductor device 50 is shown as a Pad Array Carrier (PAC) mounted onto substrate 52 with C4 technology solder bumps 53, but any other viable method of mounting can also be used. A plurality of solder bumps or balls 16, preferably of a different composition than solder bumps 23, are deposited onto the top surface of chip carrier substrate 52. The composition of solder bumps 16 can be of 60/40 Pb/Sn alloy or of another ratio. The reason for using solder of different alloy compositions on each chip carrier substrate is to facilitate rework and to prevent remelting of the solder joints in subsequent solder reflow operations. An example of a possible subsequent reflow step is the stacking of a third carrier onto the multiple chip module. Rework is also made easier because a focused beam is used to remove a solder joint. Therefore, it is desirable not to disturb the other interface of solder and substrate during the remelting of solder. In addition to solder bumps 16, which are on the top of chip carrier substrate 52, a plurality of solder bumps 15 are also deposited on the bottom surface of substrate 52. These solder bumps 16 will be used to mount the complete MCM onto a PC board, which is not shown. Again, these solder bumps should preferably be of a different composition than either solder bumps 23 or solder bumps 16, for the aforementioned reasons.

Each of the chip carriers, 42 and 48, may be tested and burned-in separately before assembling the stacked MCM. An example not forming part of the invention, a stacked three-dimensional MCM 49, is illustrated in FIG. 5. In the stacking process, the two chip carrier substrates 46 and 52 and particularly the arrays of solder bumps 16 and 23, should be aligned properly with respect to each other before solder reflow. An example of the proper alignment is shown in FIG. 1. In the solder reflow process, solder bumps 16 and 23 will coalesce to form single solder joint columns 58, as illustrated in FIG. 5. This configuration should be more reliable than solder joining two copper pins together because the top and bottom solder bumps will fuse together to form single interconnections without a weak point at the joint as in the case of the copper pins.

A variation of the present invention is illustrated in

FIG. 6. Shown is a cross-sectional view of a stacked MCM 59. A thermally conductive lid 60 has been added to the stacking configuration to form a stand-off for solder joints 29. Because of the physical restraint imposed by lid 60, solder joints 29 take on an hour glass shape which increases fatigue life for the joints because concentrated stress at the edges of the joints has been reduced.

A major advantage to the process of creating a stacked MCM is that each level of chip carriers can be assembled, tested, and burned-in prior to assembling the module. Therefore, costly rejects or using redundant chip sets can be avoided. Furthermore, rework of the present invention can be performed easily. Each solder joint or solder column can be removed and rejoined by a localized hot air technique.

The foregoing description and illustrations contained herein demonstrate many of the advantages associated with the present invention. Furthermore, it has been revealed that the configuration of this three-dimensional MCM is an efficient heat dissipating unit. The array of solder columns serve as cooling fins to aide in the natural heat convection away from the module. Thus it is apparent that there has been provided, in accordance with the invention, a stackable three dimensional multiple chip module that fully meets the need and advantages set forth previously. Dummy solder bumps could also be used for mechanical support of the lower chip carrier without affecting any of the electrical characteristics of the stacked three-dimensional MCM or the space saving advantage in the X-Y plane of the stacking configuration. Therefore, it is intended that this invention encompass all such variations and modifications as fall within the scope of the appended claims.

Claims

1. A stackable semiconductor multiple chip module (25, 59) comprising:

   a lower chip carrier substrate (26, 52) of thermally conductive material having a top and a bottom surface and a plurality of solder bumps (15) on its bottom surface;
   a first semiconductor die (10, 50) electrically and physically attached to the top surface of the lower chip carrier substrate;
   an upper chip carrier substrate (30, 46) of thermally conductive material having a top and a bottom surface;
   a second semiconductor die (10') mounted and electrically coupled to the top surface of the upper chip carrier substrate, the upper chip carrier substrate is stacked over the lower chip carrier substrate, wherein the lower chip carrier substrate and the upper chip carrier substrate are electrically connected to each other by solder joints (29); and
   a lid (28, 60) capping the first semiconductor die (10, 50) and providing a positive stand-off between both chip carrier substrates, said solder joints (29) between the upper chip carrier substrate and the lower chip carrier substrate are hour-glass shaped.

2. The semiconductor multiple chip module (25, 59) according to claim 1 wherein the lower chip carrier substrate (26, 52) and upper chip carrier substrate (30, 46) are comprised of a material selected from the group consisting of: aluminum nitride, cofired ceramic, silicon wafer material, and printed circuit board material.

3. The semiconductor multiple chip module (25, 59) according to claim 1 wherein the lower chip carrier substrate (26, 52) further comprises dummy solder bumps for mechanical support.

4. The semiconductor multiple chip module (25, 59) according to claim 1 wherein the lower chip carrier substrate (26, 52) and upper chip carrier substrate (30, 46) have through-hole vias (24).

5. The semiconductor multiple chip module (59) according to claim 1 wherein the lower chip carrier substrate (52) and upper chip carrier substrate (46) are multi-layered.

6. A method of making a stackable semiconductor multiple chip module (25, 59) comprising the steps of:

   providing a lower chip carrier substrate (26, 52) of thermally conductive material having top and bottom surfaces;
   depositing a plurality of solder bumps (15, 16) on both top and bottom surfaces of the lower chip carrier substrate;
   mounting a first semiconductor die (10) onto the top surface of the lower chip carrier substrate;
   electrically coupling the first semiconductor die (10) to the lower chip carrier substrate;
   placing a lid (28, 60) over the first semiconductor die (10) to serve as a positive stand-off;
   stacking an upper chip carrier substrate (30, 46) of thermally conductive material over the lower chip carrier substrate onto, the upper chip carrier substrate having a top and a bottom surface;
   depositing a plurality of solder bumps (23) on the bottom surface of the upper chip carrier substrate;
   mounting a second semiconductor die (10', 18) to the upper chip carrier substrate;
   electrically coupling the semiconductor die (10',

18) to the upper chip carrier substrate;
aligning the upper chip carrier substrate (30) to the lower chip carrier substrate (26) by position of the solder bumps (15, 16, 23); and
reflowing the solder bumps together to achieve physical and electrical connections (29), said electrical connections being hour-glass shaped.

7. The method of claim 6 wherein the steps of depositing solder bumps (15, 16) on the top and bottom surfaces of the lower chip carrier substrate (26, 52) and solder bumps (23) on the bottom surface of the upper chip carrier substrate (30, 46) further comprise depositing solder of different compositions.

8. The method of claim 6 further comprising the step of: attaching a heat sink (40) to the top surface of the upper chip carrier substrate.

Patentansprüche

1. Stapelbares Mehrchip-Halbleitermodul (25, 59) mit:

einem unteren Chiptträgersubstrat (26, 52) aus thermisch leitendem Material mit einer oberen und einer unteren Oberfläche und einer Vielzahl von Lothügeln (15) auf seiner unter Oberfläche;

einem ersten Halbleiterchip (10, 50), der elektrisch und physikalisch an der oberen Oberfläche des unteren Chipträgersubstrats angebracht ist;

einem oberen Chipträgersubstrat (30, 46) aus thermisch leitendem Material mit einer oberen und einer unteren Oberfläche;

einem zweiten Halbleiterchip (10'), der an der oberen Oberfläche des oberen Chipträgersubstrats angebracht und damit elektrisch verbunden ist, wobei das obere Chipträgersubstrat über das untere Chipträgersubstrat gestapelt ist und das untere Chipträgersubstrat und das obere Chipträgersubstrat elektrisch durch Lotverbindungen (29) miteinander verbunden sind; und

einem Deckel (28, 60) zum Abdecken des ersten Halbleiterchips (10, 50) und zum Bilden eines positiven Abstandshalters zwischen den beiden Chipträgersubstraten, wobei die Lotverbindungen (29) zwischen dem oberen Chiptträgersubstrat und dem unteren Chipträgersubstrat stundenglasförmig sind.

2. Mehrchip-Halbleitermodul (25, 59) nach Anspruch 1, dadurch gekennzeichnet, daß das untere Chipträgersubstrat (26, 52) und das obere Chipträgersubstrat (30, 46) aus einem Material bestehen, das aus folgender Gruppe ausgewählt ist: Aluminiumnitrid, gebrannte Keramik, Siliziumwafermaterial und Material für eine gedruckte Schaltungsplatte.

3. Mehrchip-Halbleitermodul (25, 59) nach Anspruch 1, dadurch gekennzeichnet, daß das untere Chipträgersubstrat (26, 52) weiterhin Dummy-Lothügel zur mechanischen Halterung aufweist.

4. Mehrchip-Halbleitermodul (25, 59) nach Anspruch 1, dadurch gekennzeichnet, daß das untere Chiptträgersubstrat (56, 52) und das obere Chipträgersubstrat (30, 46) Durchgangslöcher (24) aufweisen.

5. Mehrchip-Halbleitermodul (59) nach Anspruch 1, dadurch gekennzeichnet, daß das untere Chipträgersubstrat (52) und das obere Chipträgersubstrat 46 mehrschichtig sind.

6. Verfahren zum Herstellen eines stapelbaren Mehrchip-Halbleitermoduls (25, 59) mit folgenden Schritten:

Bereitstellen eines unteren Chipträgersubstrats (26, 52) aus thermisch leitendem Material mit einer oberen und einer unteren Oberfläche;

Abscheiden einer Vielzahl von Lothügeln (16) auf sowohl der oberen als auch der unteren Oberfläche des unteren Chipträgersubstrats;

Anbringen eines ersten Halbleiterchips (10) auf der oberen Oberfläche des unteren Chipträgersubstrats;

elektrisches Verbinden des ersten Halbleiterchips (10) mit dem unteren Chpträgersubstrat;

Setzen eines Deckels (28, 60) über den ersten Halbleiterchip (10), welcher als positiver Abstandshalter dient;

Stapeln eines oberen Chipträgersubstrats (30, 46) aus thermisch leitendem Material über das untere Chipträgersubstrat, wobei das obere Chipträgersubstrat eine obere und eine unter Oberfläche aufweist;

Abscheiden einer Vielzahl von Lothügeln (23) auf der unteren Oberfläche des oberen Chipträgersubstrats;

Anbringen eines zweiten Halbleiterchips (10',

18) am oberen Chipträgersubstrat;

Elektrisches Verbinden des Halbleiterchips (10', 18) mit dem oberen Chipträgersubstrat;

Ausrichten des oberen Chipträgersubstrats (30) und des unteren Chipträgersubstrats (26) durch die Position der Lothügel (15, 16, 23); und

gemeinsames Aufschmelzen der Lothügel zum Erzielen physikalischer und elektrischer Verbindungen (29), wobei die elektrischen Verbindungen stundenglasförmig sind.

7. Verfahren nach Anspruch 6, dadurch gekennzeichnet, daß die Schritte der Abscheidung der Lothügel (15, 16) auf der oberen und unteren Oberfläche des unteren Chipträgersubstrats (26, 52) und der Lothügel (23) auf der unterseite des oberen Chipträgersubstrats (30, 46) weiterhin die Abscheidung von Lot aus verschiedenen Zusammensetzungen aufweisen.

8. Verfahren nach Anspruch 6, gekennzeichnet durch folgenden Schritt:
Anbringen einer Wärmesenke (40) auf der oberen Oberfläche des oberen Chipträgersubstrats.

Revendications

1. Module multipuce semiconducteur empilable (25, 59), comprenant :

un substrat porte-puce inférieur (26, 52) en matériau thermiquement conducteur, qui possède une surface de dessus et une surface de dessous ainsi qu'une pluralité de bosses de soudure (15) sur sa surface de dessous ;
une première puce semiconductrice (10, 50) électriquement et matériellement fixée à la surface de dessus du substrat porte-puce inférieur ;
un substrat porte-puce supérieur (30, 46) en matériau thermiquement conducteur, qui possède une surface de dessus et une surface de dessous ;
une deuxième puce semiconductrice (10') montée sur le substrat porte-puce supérieur et électriquement couplée à ce dernier, le substrat porte-puce supérieur étant empilé par dessus le substrat porte-puce inférieur, où le substrat porte-puce inférieur et le substrat porte-puce supérieur sont électriquement connectés l'un à l'autre par des jonctions de soudure (29) ; et
un couvercle (28, 60) coiffant la première puce semiconductrice (10, 50) et réalisant une séparation positive entre les deux substrats porte-puce, lesdites jonctions de soudure (29) qui se trouvent entre le substrat porte-puce supérieur et le substrat porte-puce inférieur étant en forme de sabliers.

2. Module multipuce semiconducteur (25, 59) selon la revendication 1, où le substrat porte-puce inférieur (26, 52) et le substrat porte-puce supérieur (30, 46) sont constitués d'une matière choisie dans le groupe comprenant les éléments suivants : nitrure d'aluminium, céramique co-cuite, matériau pour plaquettes de silicium, et matériau pour cartes de circuit imprimé.

3. Module multipuce semiconducteur (25, 59) selon la revendication 1, où le substrat porte-puce inférieur (26, 52) comprend en outre des bosses de soudure fictives destinées à assurer un support mécanique.

4. Module multipuce semiconducteur (25, 59) selon la revendication 1, où le substrat porte-puce inférieur (26, 52) et le substrat porte-puce supérieur (30, 46) comportent des trous passants (24).

5. Module multipuce semiconducteur (59) selon la revendication 1, où le substrat porte-puce inférieur (52) et le substrat porte-puce supérieur (46) sont à plusieurs couches.

6. Procédé de fabrication d'un module multipuce semiconducteur empilable (25, 59), comprenant les opérations suivantes :

produire un substrat porte-puce inférieur (26, 52) en matériau thermiquement conducteur, qui possède des surfaces de dessus et de dessous ;
déposer une pluralité de bosses de soudure (15, 16) sur les deux surfaces, de dessus et de dessous, du substrat porte-puce inférieur ;
monter une première puce semiconductrice (10) sur la surface de dessus du substrat porte-puce inférieur ;
coupler électriquement la première puce semiconductrice (10) au substrat porte-puce inférieur ;
placer un couvercle (28, 60) par dessus la première puce semiconductrice (10) pour assurer une séparation positive ;
empiler un substrat porte-puce supérieur (30, 46) en matériau thermiquement conducteur par dessus le substrat porte-puce inférieur, le substrat porte-puce supérieur ayant une surface de dessus et une surface de dessous ;
déposer une pluralité de bosses de soudure (23) sur la surface de dessous du substrat porte-puce supérieur;

monter une deuxième puce semiconductrice (10', 18) sur le substrat porte-puce supérieur ;
coupler électriquement la puce semiconductrice (10', 18) au substrat porte-puce supérieur ;
aligner le substrat porte-puce supérieur (30) sur le substrat porte-puce inférieur (26) en positionnant les bosses de soudure (15, 16, 23) ; et
faire refondre ensemble les bosses de soudure afin de réaliser des connexions matérielles et électriques (29), lesdites connexions électriques étant en forme de sabliers.

7. Procédé selon la revendication 6, où les opérations consistant à déposer des bosses de soudure (15, 16) sur les surfaces de dessus et de dessous du substrat porte-puce inférieur (26, 52) et des bosses de soudure (23) sur la surface de dessous du substrat porte-puce supérieur (30, 46) comprennent en outre le dépôt de soudures ayant des compositions différentes.

8. Procédé selon la revendication 6, comprenant en outre l'opération suivante :
fixer un puits thermique (40) à la surface de dessus du substrat porte-puce supérieur.

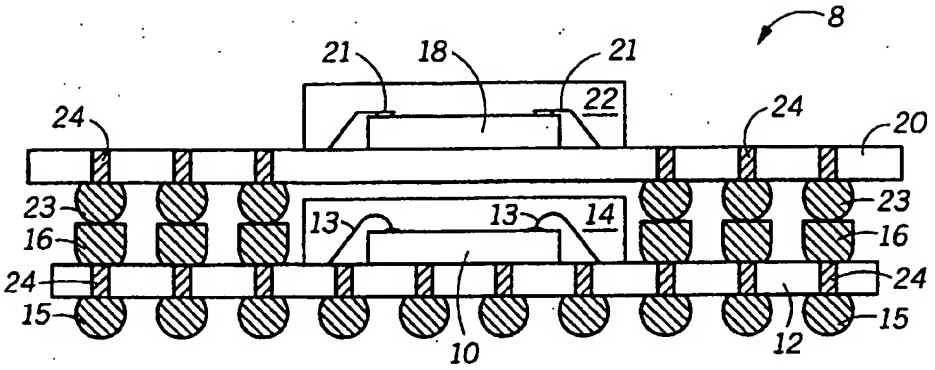

FIG.1

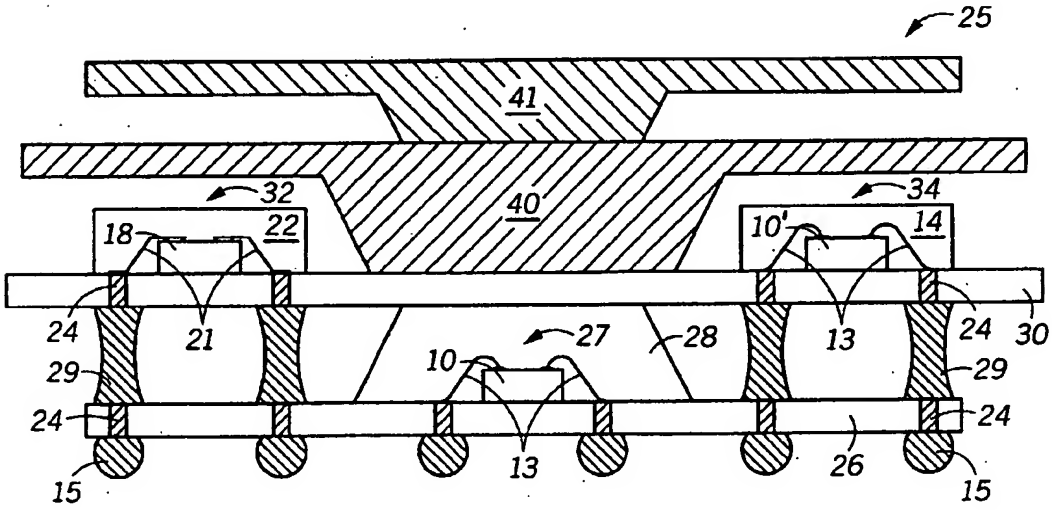

FIG.2

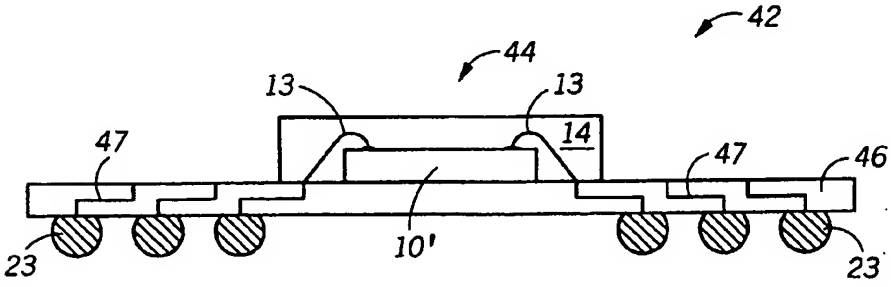

FIG.3

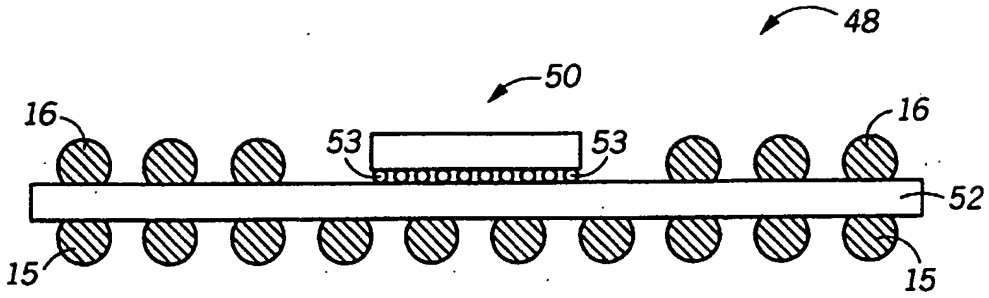

FIG.4

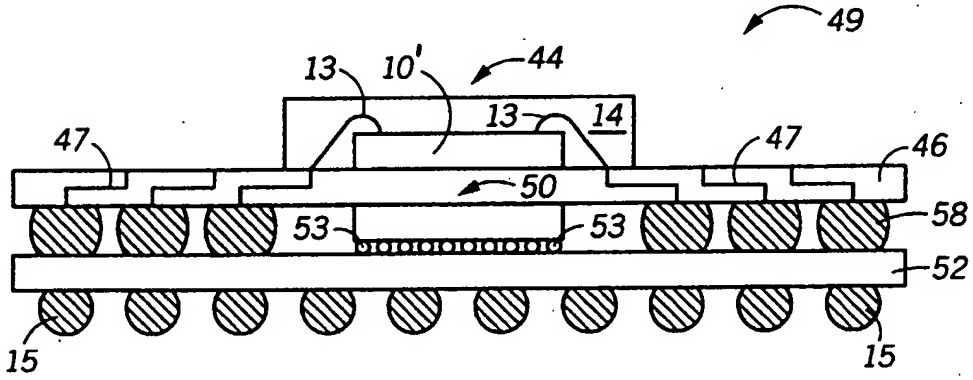

FIG.5

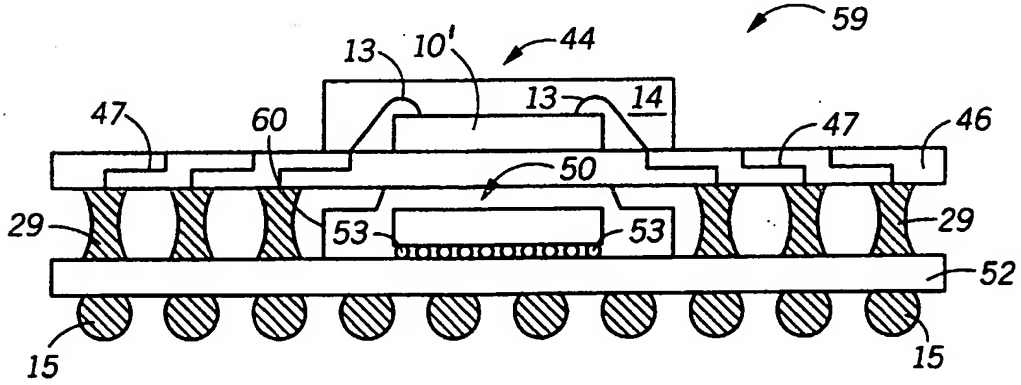

FIG.6